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Complete if Known	
Application Number	09/898,752
Filing Date	July 3, 2001
First Named Inventor	Talwar, Sunil
Group Art Unit	2124
Examiner Name	Malzahn, David

Sheet 1 of 1

Attorney Docket No: 1365.048US1

US PATENT DOCUMENTS

Examiner Initials*	USP Document Number	Publication Date	Name of Patentee or Applicant of cited Document	Class	Subclass	Filing Date If Appropriate
<i>SLH</i>	US-5,964,827 A	10/12/1999	Ngo, H. C., et al.	708	710	11/17/1997
<i>SLH</i>	US-6,175,852 B1	01/16/2001	Dhong, S. H., et al.	708	712	07/13/1998
<i>SLH</i>	US-6,269,386 B1	07/31/2001	Siers, S. E., et al.	708	710	10/14/1998

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Foreign Document No	Publication Date	Name of Patentee or Applicant of cited Document	Class	Subclass	T ²
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OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
<i>SLH</i>		BEDRIJ, O. J., "Carry-Select Adder", <u>IRE Trans., EC-11</u> , (June 1962),340-346	
<i>SLH</i>		KNOWLES, S. , "A Family of Adders", <u>Proc. 14th IEEE Symp. on Computer Arithmetic</u> , (1999),30-34	
<i>SLH</i>		KOGGE, P. M., et al., "A Parallel Algorithm for the Efficient Solution of a General Class of Recurrence Equations", <u>IEEE Trans. Computers</u> , Vol. C-22, No. 8, (Aug. 1973),786-793	
<i>SLH</i>		LADNER, RICHARD E., et al., "Parallel Prefix Computation", <u>Journal of ACM</u> , Vol. 27, No. 4, (Oct. 1980),831-838	
<i>SLH</i>		LING, HUEY , "High-Speed Binary Adder", <u>IBM Journal of Research and Development</u> , Vol. 25, No. 3, (1981),156-166	
<i>SLH</i>		SKLANSKY, J. , "Conditional-Sum Addition Logic", <u>IRE Trans., EC-9</u> , (June 1960),226-231	
<i>SLH</i>		WEINBERGER, A. , et al., "A Logic for High-Speed Addition", <u>Nat. Bur. Stand. Circ.</u> , 591, (1958),3-12	

EXAMINER

D. H. Malzahn

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Substitute Disclosure Statement Form (PTO-1449)

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